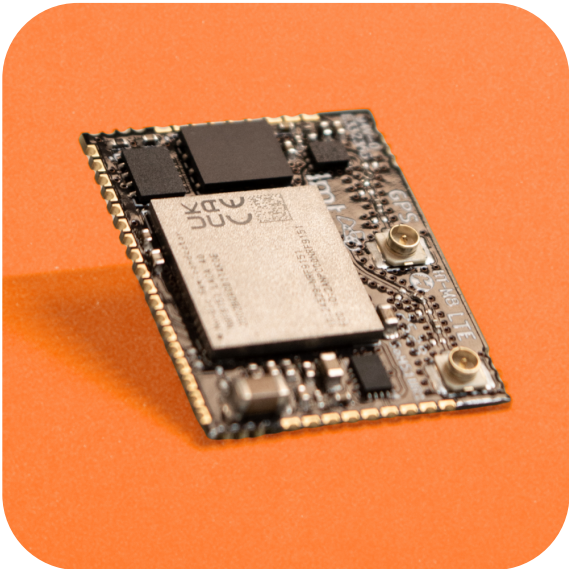


LMT LTE-M/NB-IoT System-on-Module

As the hardware core of the **LMT IoT Shortcut** ecosystem, this System-on-Module (SoM) accelerates cellular IoT deployment. It features LTE-M/NB-IoT connectivity via a built-in global SIM and is optimized for ultra-low power consumption. Beyond hardware described in this datasheet, the solution integrates a specialized SDK and native LMT IoT Cloud compatibility to streamline cellular IoT design and deployment.



1 Ordering Information

		Packaging type	
Antenna implementation		Tape-and-Reel	Tray
External antenna		SOM51U10TR	SOM51U10TY
Chip antenna		SOM51C10TR	SOM51C10TY

The listed products feature a castellated-pin PCB design suitable for either SMT assembly or hand soldering. They are available in tape-and-reel packaging (350 pcs/reel) or trays (50 pcs/tray) for SMT assembly, as well as individually bagged items (10 pcs/box) for smaller hand-soldering batches. Alternative form factors (such as M.2 connectors or pin headers) and custom packaging options are available upon request.

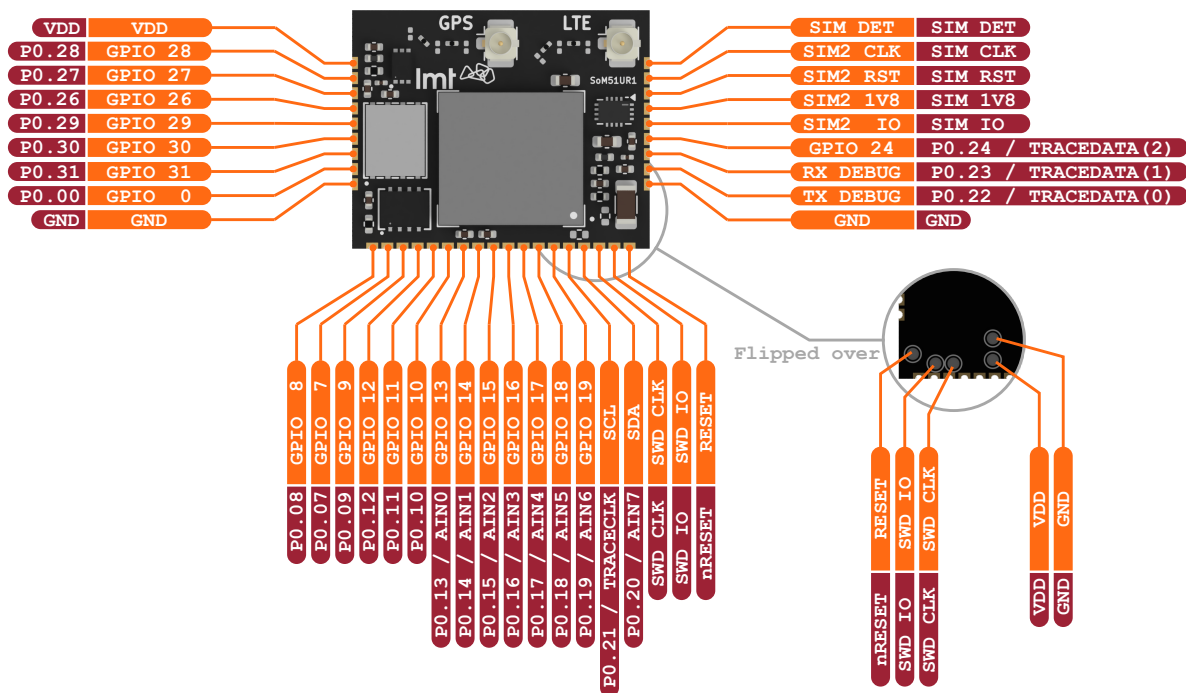
2 Technical Specifications

Main modem/MCU	Nordic Semiconductor nRF9151
Connectivity	LTE-M (Cat-M1), NB-IoT (Cat-NB1/NB2), NB-NTN (satellite IoT), GNSS (GPS)
Operating voltage	3.2–3.6 V (Absolute maximum range 0.0–3.9 V)
Deep sleep current consumption	<8 µA at 3.6 V supply
Single upload energy consumption	90 mJ or 25 µWh (100 B payload, excellent signal)
Application processor	64 MHz ARM Cortex-M33
Processor memory	1 MB flash and 256 KB RAM
RF output power	Up to +23 dBm (Power Class 3) and +20 dBm (Power Class 5)
Digital peripherals	I ² C, SPI, UART, I ² S
Analog peripherals	7×12-bit 200 ksps, 4×PWM units
External memory	4 MB flash

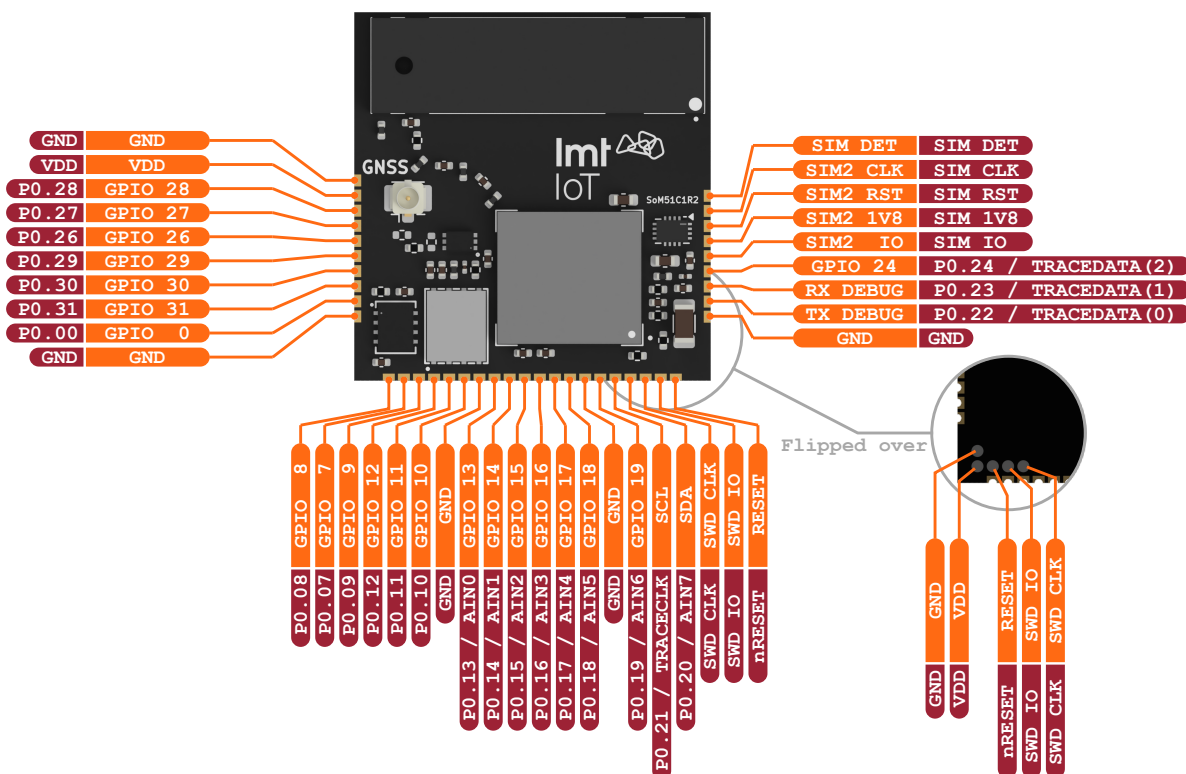
3 Pin Configuration

The images below display pinout diagrams for both available PCB implementations of the LMT SoM. LMT pin designations are shown in orange, but nRF9151 documentation designations are in red.

3.1 External Antenna Version



3.2 Chip Antenna Version



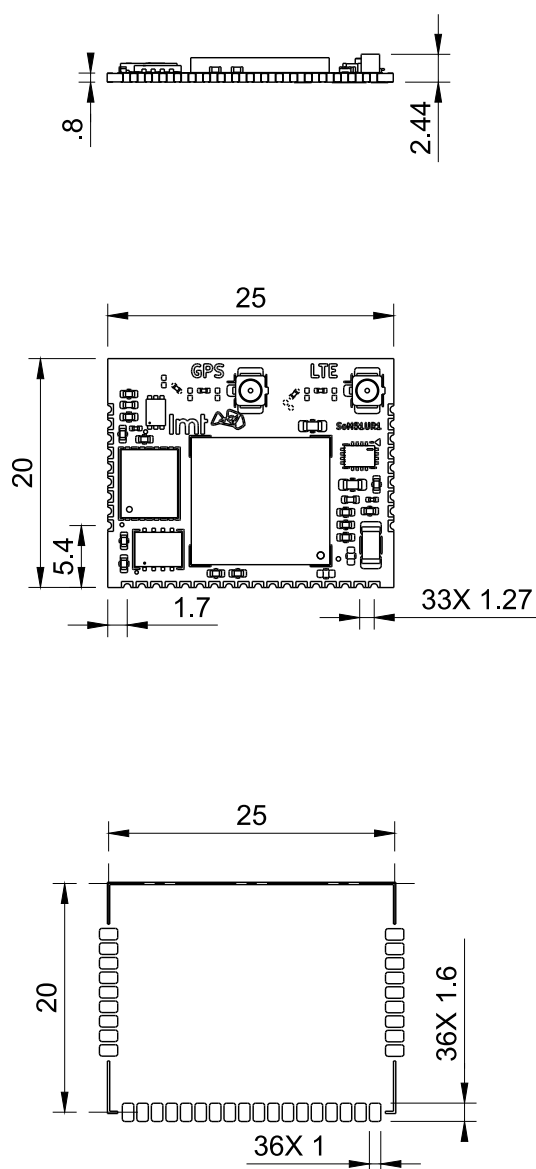
4 Mechanical Dimensions

The LMT SoM comes in two variants (external or chip antenna), both using a castellated pin configuration for SMT assembly or manual soldering. The physical dimensions and recommended soldering land patterns for each version are displayed below (.step file downloads — [external antenna](#) and [chip antenna](#) versions). **All dimensions are in mm.**

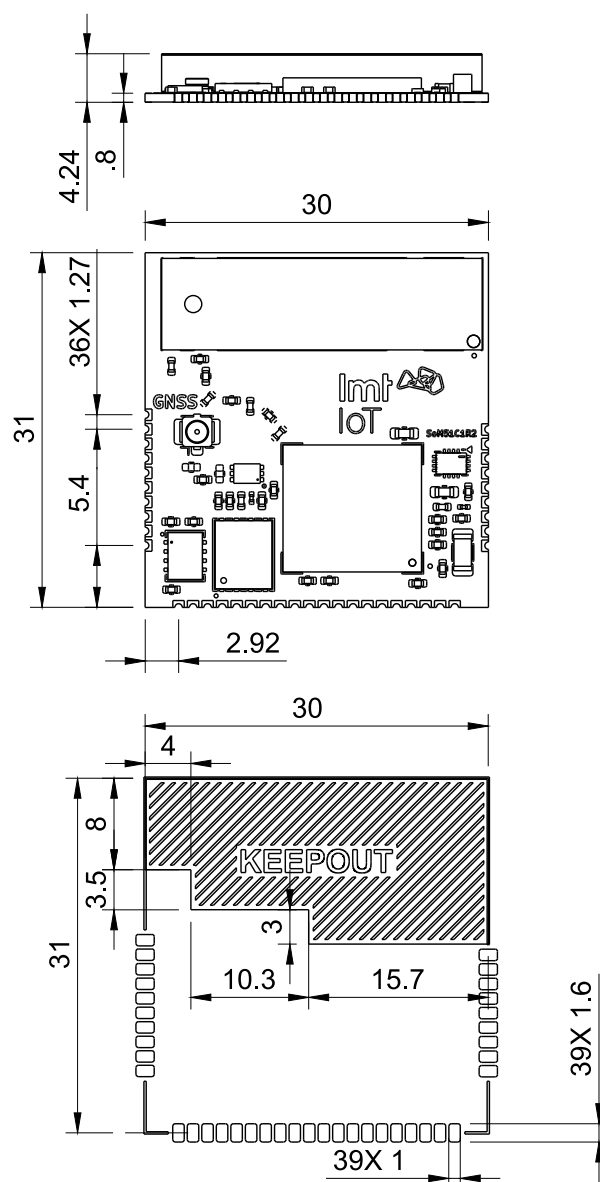
The chip antenna version serves as a self-contained RF solution, integrating an onboard chip antenna within a 30×31 mm footprint. When integrating this version, designers must note the keepout zone designated in the blueprint; this specific area must remain free of copper, ground planes, and components on all layers of the host PCB to ensure the antenna functions with optimal radio efficiency.

For designs where space is at a premium or external antennas are required, the UF variant offers a reduced form factor of 20×25 mm with a lower vertical profile. This model substitutes the onboard antenna with standard U.FL connectors for both LTE and GPS interfaces, allowing the module to fit into tighter enclosures while routing RF signals to chassis-mounted antennas.

4.1 External Antenna Version



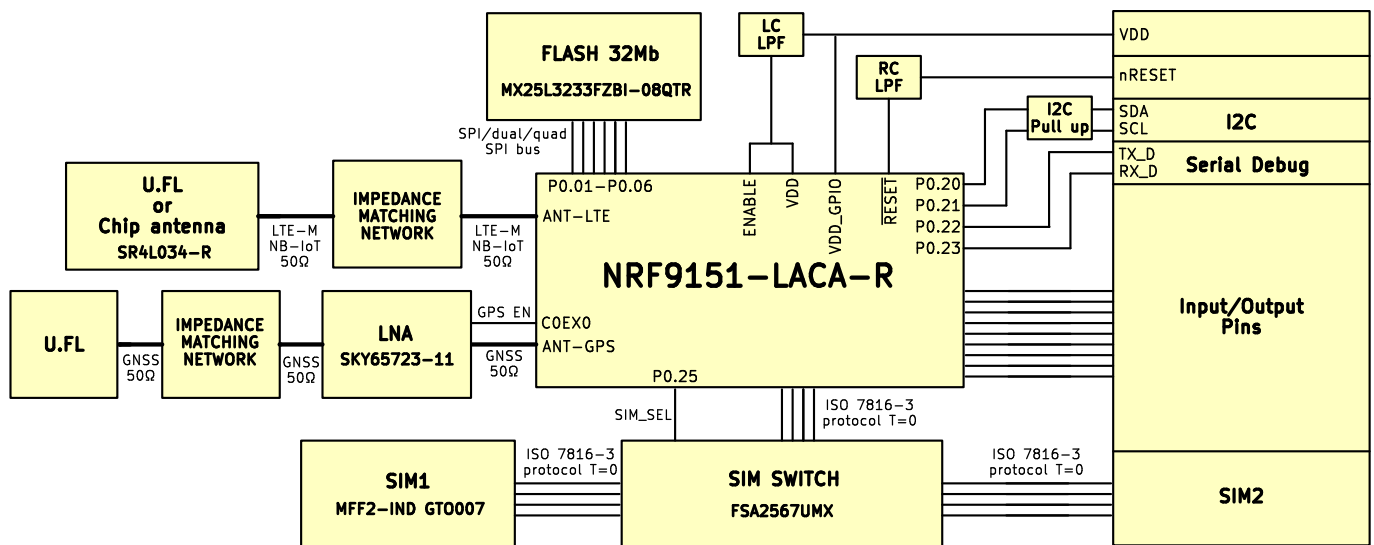
4.2 Chip Antenna Version



5 Functional Block Diagram

The LMT SoM architecture is based on the Nordic Semiconductor nRF9151 System-in-Package. The RF design features split paths for cellular and GNSS connectivity. The LTE-M/NB-IoT interface connects via an impedance matching circuit to either an onboard chip antenna or an external U.FL connector. The GNSS path receives input from a dedicated U.FL connector, which routes through a low noise amplifier (LNA) before entering the modem.

Onboard peripherals include an external flash memory connected via a Quad SPI bus. A dual-SIM topology utilizes an SIM switch to toggle between the embedded MFF2 SIM and an external SIM interface, controlled by the SIM_SEL line. External I/O includes an I2C bus with integrated pull-up resistors and a UART serial debug port.



6 Application Notes

6.1 RF and Antenna Guidelines

- Both the GNSS and LTE RF paths are designed for 50 Ω impedance. The U.FL antenna must be selected to provide an impedance match across the intended frequency bands to ensure maximum RF performance. The GNSS input is designed for passive antennas only; do not apply DC power or use active antennas on this port.
- For the SoM with chip antenna: placement on the board, correct ground connections are critical for good RF performance. Place the SoM in the upright position in the top right corner of the board, maintain the antenna keep-out area also to the right and above SoM (no copper or components inside the keep-out area). For optimal performance, do not place the antenna or carrier PCB next to metal objects or in a metal case.
- The current chip antenna matching network is designed for a 75 $\times$ 75 mm, 2-layer, 1.6 mm PCB. Smaller boards are not recommended when using the chip antenna version of the SoM. If the carrier board size is drastically different, the matching network values might need to be changed. For more information about the antenna and its placement, refer to [Antenova Inversa SR4L034 chip antenna documentation](#).

6.2 Power and Low-Power Design

- During transmit (TX) mode, current pulses can reach up to 500 mA, while the average current is around 40 mA.
- We advise adding a low-ESR (<100 m Ω) 100 μ F bulk capacitor and a power supply that can deliver at least 300 mA

while maintaining rated supply voltage. Additional decoupling capacitors can be added for supply stability close to VDD pin.

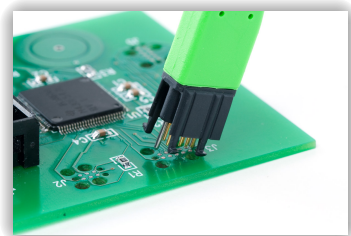
- Reset pin is connected to internal RC debounce circuit (series 1 k Ω resistor and grounded 100 nF capacitor), but additional firmware debounce is recommended.

6.3 Communication and GPIO

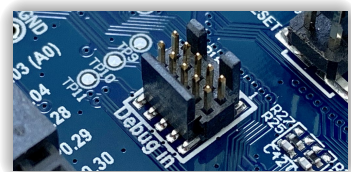
- I²C pins support up to 400 kHz communication using 10 k Ω pull-up resistors.
- Pull-up resistors for the I²C lines are already integrated for the chip antenna version. However for the U.FL version, pull-up resistors must be integrated on the carrier board if I²C functionality is required.
- SWD programming/debug signals (SWD IO, SWD CLK) should be routed short and direct, isolated from high-speed noise, and only driven when the SoM is powered.

6.4 Notes on Firmware Programming

- By default, the module is shipped without firmware. The customer is responsible for developing and flashing the application firmware onto the end product during the manufacturing process. Pre-flashing services for custom firmware are available upon request; please contact us for details.
- For production firmware flashing, it is highly recommended to route the nRESET, SWDIO, SWDCLK, VDD, and GND pins to Tag-Connect pads. Utilizing an SWD interface with spring-loaded pogo pins (such as the **TC2030-CTX** or the space-saving **TC2030-CTX-NL**) minimizes the required PCB footprint and is ideal for high-volume manufacturing using programming jigs.
- For applications where manual flashing is preferred and PCB space is not a strict constraint, a standard 10-pin (2x5, 1.27 mm pitch) JTAG/SWD header may be utilized as an alternative.
- **Segger J-Link** debug probes are recommended for all firmware flashing and debugging operations.



(Use of TC2030-CTX connector)



(Use of SWD connector)